ABSTRACT

According to one embodiment, an apparatus for detecting and preventing tampering with a programmable digital device. The apparatus comprises a one-time programmable (OTP) memory that includes a plurality of memory cells to store data. The plurality of memory cells may be programmed to a default state or a state opposite the default state. A tamper detection circuit is coupled to these memory cells in order to sense a condition when each bit associated with the plurality of memory cells is programmed to the state opposite the default state. In response to detecting this condition, it is considered that the programmable digital device implemented with the apparatus has been tampered with and operations are performed to combat the tampering of the digital device.